Timothy S. Cale, Ph.D.

timothy.cale@gmail.com, 480-381-2228, www.process-evolution.com

Objective

Provide software tools and consulting services that improve materials and processes.

Summary

I have extensive experience identifying opportunities, securing funding, establishing facilities, assembling teams, defining targets, and monitoring accomplishments. I have established materials fabrication and testing laboratories, processing facilities, and process and materials simulation efforts in both industry and academia. One of my key roles in academia and industry has been to explain the purpose, progress, and potential of projects to investors, collaborators and customers. In addition to satisfying stakeholders, I focus on developing people.

References and/or more details are available on request. For an "academic CV", visit www.process-evolution.com, then follow "Contact PE", "Timothy S. Cale", "CV".

Education

Ph.D. Chemical Engineering, University of Houston, 1980

My dissertation was on heterogenous catalysis, and involved fabricating, characterizing, and testing catalysts, with a focus on magnetic, adsorptive, and kinetic characterizations.

B.S. Chemical Engineering, Arizona State University, 1976 (summa cum laude)

Experience

Industrial (post-BS):

2014 - 15 CTO, reNatue, Inc.
2011 - 15 Board Member and Advisor, reNature, Inc., focused on a sustainable nutrient cycle
2008 - 11 CTO, Ambature, LLC , a startup focused on novel high conductivity materials
1997 - Principal, Process Evolution, Ltd., a software and consulting company
1991 - 97 Motorola, summers, a sabbatical year and a year as the ASU assignee in a leadership exchange program
1986 Process Engineer, Intel Corp. (summer)– introduced me to IC fabrication
1976 Process Engineer, Monsanto Company – introduced me to petrochemical processing

Academic:

2007 - 12 Research/Adjunct Professor, Arizona State University
1998 - 07 Professor of Chemical Engineering, Rensselaer Polytechnic Institute
1998 - 04 Director, Focus Center - New York, Rensselaer: Interconnections for Hyperintegration
1993 - 95 Director, Center for Solid State Electronics Research, ASU
1981 - 97 Professor of Chemical Engineering, ASU (Asst., Assoc., Full)

Selected Leadership Contributions

Industrial:

As Chief Technology Officer of Ambature, LLC, I worked with corporate leadership and investors to establish technical goals that also served as milestones for increases in company valuation. I provided day-to-day management of a diverse technical team, from technicians to Ph.D.s, and I educated personnel on aspects of superconductivity that are relevant to Ambature. I also taught the group the methods needed for data acquisition and analysis, including sensing and control during dynamic tests. I joined the company as employee No. 4, when there were no physical facilities. I led the effort to build the technical team, and to establish a laboratory in which novel superconductor materials are fabricated, characterized, and tested. In order to expand our capability, increase our versatility, and improve our ability to validate progress, I drove the development of a relationship with Arizona State University. I worked with Ambature's CEO and ASU personnel to handle IP, access, and security issues related to Ambature performing R&D in ASU facilities. Ambature has several employees stationed at ASU, where they have access to state of the art equipment to fabricate, characterize, and test materials. I also initiated a materials modeling effort to predict materials properties relevant to superconductivity. The value of Ambature soared due to the accomplishments of my technology team. In addition to technical management, I helped write patents, met with investors and stakeholders, and pursued relationships with potential collaborators and customers.

My leadership position in semiconductor related process modeling and simulation (described below) led to my helping to define new areas of research in both academia and industry. In particular, I have helped industrial development groups improve processes, and to integrate processes, associated with IC fabrication and the integration of ICs with sensors. This work resulted in specific recommendations regarding process changes. More important than those specific recommendations are my contributions to establishing improved methodologies for process understanding and improvement.

Academic:
I achieved research success as a faculty member by, both individually and in collaboration with others, identifying research opportunities, proposing novel projects subject to peer review, and executing the proposed research using appropriately staffed research teams. I demonstrated the ability to work with colleagues and funding agencies to define research areas and to ensure research impact, stakeholder satisfaction, and continuation of funding.

I helped develop funding initiatives and foci for several funding agencies and programs. In addition to meetings with federal funding agencies to define research program, I served on the University Advisory Board of the Semiconductor Research Corporation (SRC), with the role of advising the SRC on university funding priorities needed to achieve goals established by the International Technology Roadmap for Semiconductors.

I directed the Center for Solid State Electronics Research (CSSER) at ASU. CSSER was supported by Arizona to facilitate solid-state electronics research, broadly defined. A large part of this position was essentially business development. Center personnel helped acquire and facilitate the execution of millions of dollars per year of research funding. The facilities included a clean room, as well as multi-project processing, testing, and simulation tools. In addition to managing and improving the operations of CSSER, I worked with the Dean of Engineering at ASU to improve the relationship between ASU and the local microelectronics industry. For example, we brought in Motorola personnel to jointly direct CSSER, which led to several years of strong industrial input, and increased collaborations with other local companies. I also worked with the Dean and industrial colleagues to initiate a broad upgrade of semiconductor materials processing facilities at ASU, which was particularly aided by industrial donations of processing equipment and expertise of experienced industrial colleagues.

I directed the “Focus Center – New York, RPI” (FC-NY, RPI) at RPI, which was supported by the Semiconductor Industry Association (SIA), Defense Advanced Research Projects Administration (DARPA), New York State (NYS), and several IC manufacturing companies. The FC-NY, RPI was part of a nationally distributed research effort, called the Interconnect Focus Center (IFC), which sought to overcome barriers to improved performance of interconnects in ICs. Major contributing universities in the IFC were Georgia Institute of Technology (lead), MIT, Stanford, SUNY-Albany, and RPI. The FC-NY, RPI worked closely with Albany Nanotech, an increasingly important hub in the world of nanotechnology. I managed a multi-million dollar per year portfolio of projects with the goal of developing materials and processes, as well as materials, process, and device simulation, which advance the design and fabrication of IC interconnects. As a leader of the IFC, I participated in defining the international research and development agenda relative to IC interconnects. A large part of my position was business development; i.e., I established relationships with companies to promote our research agenda. The RPI team of faculty, post-docs, and students developed several key solutions to interconnect hurdles, and kept the research sponsors and stakeholders satisfied.

Professional:

I served on program committees of many international conferences and symposia, both specialized, and as part of my membership in professional and technical societies, AIChE, MRS, AVS, IEEE and ECS. Essentially, I helped define the conferences; i.e., what was important to the stakeholders.

I presented keynote and invited talks at many international conferences and symposia, and I am co-author of hundreds of papers and hundreds of presentations.

I served on international teams to evaluate research proposals for funding decisions, both for individual research groups and for large research centers.

I offered short courses focused on improving students’ understanding of fundamental transport and reaction processes, and the impact of process setpoints on changes in wafer state. These courses included topics in multiscale and multiphysics modeling.

I see the guidance of graduate students through their degree program as a professional leadership contribution. I have advised more than 50 students who are contributing through jobs in industry, academia and government.

Selected Technical Contributions

I have established several materials processing and characterization laboratories. The materials processed and tested in these laboratories range in scale from milliliters of catalysts and specialized centimeter scale equipment, to silicon wafers processed in industrial scale equipment. I have also written materials and process software and led teams to develop software.

My first major research area, pursued at ASU, was heterogeneous catalysis. Catalysts are used to carry out chemical reactions that are central to our quality of life; e.g., to manufacture everyday products, in energy conversion, and in environmental engineering. The catalyst temperature in the chemical reactor determines chemical reaction products and safe reactor operation. My research team developed the first method to determine the temperature of “supported” heterogeneous catalysts, which in this case consisted of nanometer scale pieces of metal distributed in a ceramic matrix. The temperature of these pieces of metal cannot be measured by normal methods because of their size. We demonstrated how our unique magnetic method might be used to safely produce chemicals more efficiently, by running the reactors under control at higher conversion levels. The ability to measure catalyst temperature also provides a method that can be used in fundamental engineering research to improve the transport and reaction models used to design and operate chemical reactors.

Microelectronics was my second focus of research and teaching. At both ASU and RPI, I was a leader in the development of our understanding of key aspects of IC manufacturing. I helped improve IC fabrication by highlighting the roles of chemical reactions in process steps, and by relating equipment design and operating setpoints to events on the nanometer scale. Below are examples of my technical contributions in the area of semiconductor processing. For others, see my academic CV, which can be accessed as described on page 1 of this document.

A major obstacle to fabricating ICs is accomplishing the desired changes at the nanometer (or “feature”) scale during each process step. This motivated a research field called “topography evolution”, to which I made significant contributions. While at ASU, I introduced a model that explained how feature surfaces evolve in shape and composition during many processes used to fabricate ICs, such as low-pressure deposition and etch processes. I worked with others who developed models for reaction chemistry to demonstrate previously unexplained topography evolution during critical processes. My “ballistic transport and reaction model” formed the basis of software named EVOLVE, which has been used by most major IC manufacturers. I held technology transfer courses to teach colleagues from industry, national labs, and academia on the basis and uses of EVOLVE. EVOLVE has been used to optimize IC fabrication processes, by relating process physics and chemistry to the resulting changes in wafer state. One example application of this feature scale modeling was the prediction that the throughput of chemical vapor deposition processes could be improved by changing the temperature in a prescribed manner during processing. We experimentally validated this “programmed rate chemical vapor deposition” concept a few years after the prediction was made. More generally, the approach to modeling surface evolution used in EVOLVE and its extensions have become standard practice in the IC industry, and topography evolution is no longer a significant research area.

Another hurdle to IC manufacturing is uniformity of processing; high uniformity is needed so that all of the ICs are very similar, from wafer to wafer and on each wafer. At ASU, I worked with a multi-disciplinary team of academic and industrial colleagues, including mathematicians, electrical engineers, and material scientists, to demonstrate the first fully multi-scale, multi-physics model that relates equipment scale design and setpoints to phenomena on the wafer scale, die scale, and nanometer/feature scale. We used mathematical homogenization to combine in-house software (EVOLVE) and commercial finite element software to study deposited film uniformity at the wafer scale, die scale and feature scale, including a phenomenon known as “pattern density effects” or “loading”. Our method can be used by design and process engineers with existing engineering software to help design processing equipment, establish operating conditions, and control processes in order to consistently produce high quality ICs.

Chemical mechanical planarization (CMP) has been central to the development of ICs with improved performance at lower cost, but the process was not well understood for several years after its introduction into manufacturing, so development was largely trial and error. At ASU and RPI, I worked with academic and industrial colleagues to improve our understanding of CMP. Our work helped explain the roles of chemistry, stresses, and temperatures in CMP. Colleagues in this area of research have extended our research, and have applied their understanding to improve equipment design, operating conditions, and control. For example, this understanding helps engineers prescribe how process conditions should be programmed during CMP in order to improve throughput and results.

The detailed microstructures of polycrystalline materials in ICs impact their performance and reliability. My research groups at ASU and RPI developed a “grain-focused” model and associated software (PLENTE) that represents and tracks grains in polycrystalline films in three dimensions (3D). In one study the team used materials models, PLENTE, and commercial multi-physics software to demonstrate that grain-focused models provide computed results that differ significantly from computed results when “continuum” models of materials are used; e.g., the distribution of thermally generated stresses. This study provides guidance as to how companies can establish more reliable IC design windows; e.g., target dimensions in interconnect structures. We also used PLENTE to demonstrate the evolution of copper grains in interconnects, with computed results that are in reasonable agreement with experimental results. This study provides companies with an approach to studying the reliability of interconnect structures. Our methods are being extended and combined with other grain-focused approaches to improve materials models in microelectronics, as well as other domains.

A key driver in the microelectronics industry for several decades has been “Moore’s Law”; i.e., increased functional density in ICs. At RPI, we had the foresight to establish research projects to develop ICs with multiple layers of active devices (called 3D-ICs). As Director of the FC-NY, RPI, this research program was part of my portfolio, and I participated in the program as a member of an academic, industrial, and government team that helped initiate worldwide research and development in 3D-ICs. Our 3D-IC process research team demonstrated ways to interconnect wafers that contain previously fabricated ICs. In one project, our 3D-IC simulation team used thermomechanical modeling, including our in-house, grain-focused code (PLENTE), to establish design windows to guide the development of stable, reliable 3D-IC interconnects. Some of the approaches that we developed have been adopted and extended in the IC industry. 3D-ICs are actively being developed because they are seen as one way to continue the push towards increased functional density, as delineated by Moore’s Law.